

1. (Twice amended) A process for manufacturing an integrated circuit package comprising:

b1 (a) forming a substrate having a first dielectric layer, a conductive layer having a first region insulated from a second region and located above the first dielectric layer, and a second dielectric layer above the conductive layer, the second dielectric layer having a cavity wherein the first and second regions are exposed within the cavity and the first region insulated from the second region by a third dielectric layer; and

(b) interconnecting a first lead of an integrated circuit to the exposed first region and interconnecting a second lead of the integrated circuit to the exposed second region.

(2) Please amend Claim 7 as follows:

7. (Twice amended) A method of manufacturing a substrate adapted to receive an integrated circuit chip comprising:

b2 (a) forming a first dielectric layer on a substrate;

(b) forming a conductive layer having a first region insulated from a second region, above the first dielectric layer;

(c) forming a second dielectric layer above the conductive layer; and

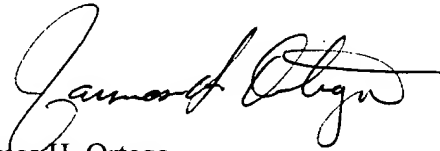
(d) forming a cavity in the second dielectric layer to expose the first and second regions of the conductive layer and coupling a first lead of the integrated circuit chip to the exposed first region and coupling a second lead of the integrated circuit to the exposed second region, the first region insulated from the second region by a third dielectric layer.

**REMARKS**

The Applicants have carefully reviewed the cited references and respectfully submit that the pending claims are allowable. Therefore, a Notice of Allowance for Claims 1-16 is respectfully requested.

Should it facilitate allowance of the Application, the Examiner is invited to telephone the undersigned Attorney of Record. The Commissioner is hereby authorized to charge any additional payment that may be due or credit any overpayment to Deposit Account No. 08-2395.

Respectfully submitted,  
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